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ERROR SOURCES IN ANALOG ASICS AND WAYS FOR THEIR MINIMIZATION

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ABSTRACT

This paper is dedicated to the analysis of analog application specific integrated circuits (ASIC) possible error sources and how they can be effectively overcome. This is done in order to obtain a precondition for building up an analog ASIC development methodology which would utilize the error minimization techniques and thus would be applicable to be used in the corresponding product design for safety-critical applications. For the reason to keep the exposition in a systematic order there will be 2 main parts in the paper. The first part will present the main sources of errors in analog ASICs. In the second part ways to minimize the effects of these errors will be considered.

Keywords: ASIC; error source; design

I. INTRODUCTION

The fast growing electronic systems' complexity requires an increased number of functions integrated in a single product, which size keeps on shrinking. This manifests in chips' integration increase. The most spectacular example of such integration is found in system-on-a-chip (SOC) approach where different functions are integrated on a single chip instead of using several discrete devices. This approach changed the entire design concept. If earlier manufacturers released standard products, which were used by the customers as building blocks for their systems, now SOC products are done specifically for each customer with the regard of their parametric needs. Thus the products received the name "Application Specific Integrated Circuit" or ASIC.

Historically the first ASICs were purely digital, however later analog ASICs were also introduced. An example of analog ASIC can be found in power management application for portable products, where a single-chip power management unit works as a multiple energy converter, taking energy from a single source such as battery and transforming it to different levels to provide each type of peripheral device with the suitable one.

As the complexity and integration of such devices is high, they encounter more specific error sources in addition to the ones present in conventional discrete devices, making them more prone to critical failures. Current article will address the most widespread error sources of both types and try to work out methods for overcoming them.

As it has already been said earlier the entire paper will consist of error sources analyses part and the techniques for error minimization part. However each of them in its turn will be divided into smaller sections grouped by the types of error sources or minimization techniques. It is hard to radically isolate each section from each other, because many of them have common features and are tied together in one way or another so in some parts this division may seem formal, but in any case it should perform its main task of systemizing the exposition so that it is easier to understand.

II. THE SOURCES OF ERRORS

In this chapter the main ASIC error sources, both common for all analog ICs and specific ASIC ones, will be named and analyzed. First a group of errors which can be named as physical errors will be considered. This will be followed by examination of design errors. After that technological or process error sources will be overviewed.

2.1 Physical Errors

This is a standalone type of error source which on one hand can be present in all other source types, but on another hand cannot be placed in well constructed hierarchy of other sources. Temperature and electrical noise are the best known physical error sources and they can be of 2 types: internal and external. If external ones like electromagnetic interference from RF waves, switching disturbance and ambient temperature rise can be more or less easily isolated by shielding materials, the internal sources cannot be overcome that easily. That is why main concentration here will be made in favor of the latest.

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2.1.1 Temperature based internal error source

All circuits not depending on their complexity have some kind of equivalent resistance which can be dependent on different factors such as working modes or can be constant. This means that when a current (I) passes through this resistance (R), power (P) is dissipated over it which results in heat generation (Q) as shown in (1) and (2):

$$P=I^2R, \quad (1)$$

$$Q=P\Delta t. \quad (2)$$

Δt in (2) represent the time period during which the power was dissipated inside the resistance.

Moreover this heat generation can vary in time and space meaning that temperature can fluctuate inside the chip creating temperature gradients over the chip area. There are 2 main causes for such non-uniformity.

a) The physical discontinuity of applied voltage and current: This means that each device starting from the smallest transistor cannot have a constant voltage on any of its node. An example can be seen in Fig. 1. Here the current is slightly more intense to the center of the channel due to the smaller voltage drop between drain and source in this region [1].

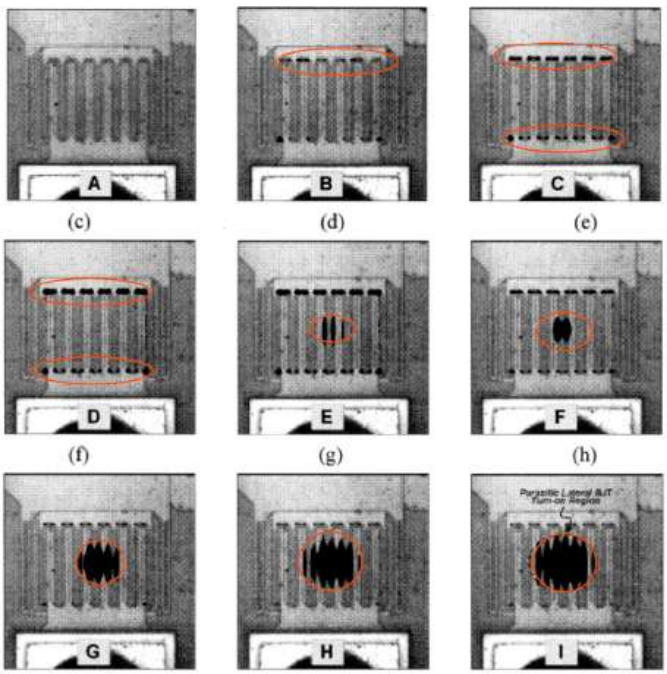

Figure 1. Photon generation of the NMOS under direct voltage.

b) Temperature fluctuation from circuit's complexity: This is a specific problem that is encountered in analog ASICs. Many functions that are integrated into these devices are needed only in certain moments and are not system critical. Thus they are switched off at the time when their function is not needed. This turning on and off of different blocks brings a rise in temperature fluctuations in entire chip in a weakly determining way.

The problems that can bring temperature drift lay mainly in component's performance plain. For example it can affect resistor's resistance or the threshold voltage (Vth) of a MOSFET, which can significantly affect the performance of different blocks and the entire system. In critical cases, the excessive heat can cause thermal breakdown of the device.

2.1.2 Circuit generated electrical noise

The definition of electric noise states that it is a random, usually unwanted fluctuation of voltage or current in a conducting material, caused by different sources. Internal circuit's noise can be of 4 types: thermal noise, shot noise, flicker noise and burst noise.

c) Thermal noise: Is due to random thermal motion of carriers (electrons and holes) in semiconductor. This motion is present always when there are free carriers and the material's temperature is above 0K. Because of their chaotic movement carriers cause unwanted voltage and current fluctuations which average value is 0 however at a random point of time they can have values which differ from 0. Thermal noise does not depend on applied signals and has white noise frequency spectrum. Power spectral density is linearly proportional to absolute temperature and can be found in (3):

$$v^2(f)=4kTR. \quad (3)$$

where k is Boltzmann's constant, T is absolute temperature and R is ohmic resistance of the material.

d) Shot noise: Results from discrete movement of charge, which is more visibly present when carriers pass a potential barrier, meaning that although the average net charge passed through a particular cross section is constant the momentarily charge may vary because it is conducted by separate electrons and holes. This type of noise is present only when there is a direct movement of charge resulting in electric current, which is present when voltage is applied to semiconductor. Power spectral density of this noise type can be expressed in (4):

$$i^2(f)=2qI_{DC}. \quad (3)$$

The frequency spectrum noise of shot noise is similar to thermal one, which means that it can be regarded as a white noise source.

e) Flicker noise: Physically this noise can be caused by traps associated with impurities and crystal defects. The traps randomly capture and release charge carriers giving the rise of the noise magnitude which is inversely proportional to frequency, meaning that it is significant on lower frequencies and overshadowed by white noise on higher frequencies like shown in Fig. 2. Like shot noise, flicker noise is also present only when an external voltage is applied [2, 3].

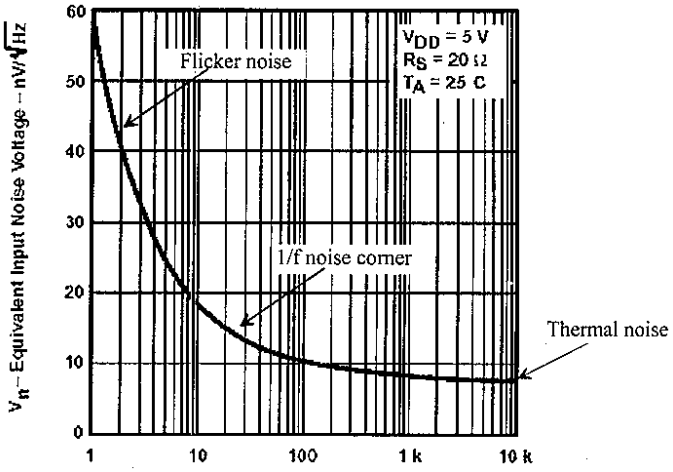

Figure 2. Noise frequency spectrum of a real semiconductor device.

f) Burst noise: The nature of this noise is not completely studied and understood, however the most likely reason for it is intense contamination of semiconductor by heavy metals such as gold. These polluted zones catch passing carriers for a period of time giving a rise to space charge. This charge is released at a random point of time resulting in an energy spike. These energy spikes shown in Fig. 3 are the burst noise components [2, 3].

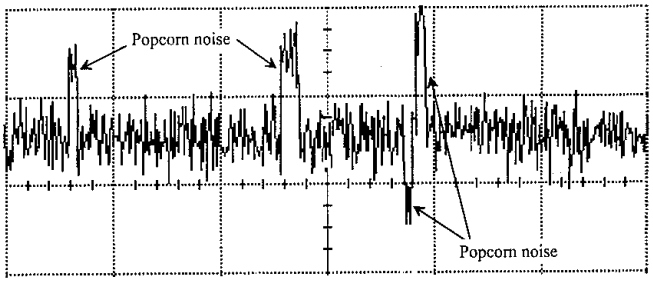

Figure 3. Burst noise waveform.

2.2 Design Errors

Errors based on design inconsistency are ones of most importance in the entire error source spectrum, as the consequence from these errors may be dramatic resulting in the critical failures of ASICs. Design errors can occur on both block and system level and although system encounter all the same errors present in the blocks, there are additional specific error sources which are relevant to large systems only.

2.2.1 Block design errors

These are common error sources for all integrated circuits starting from standard single block products like amplifiers or low dropout regulators (LDOs) and finishing with highly integrated ICs like very large scale integration (VLSI) SOCs. These errors include all kinds of miscalculation and rules' abuse.

a) Calculation errors: One possible error source is parameter or variable miscalculations which together with design algorithm inaccuracy build up a group which can be named human caused design errors. These are designer's errors and can be of random consequence, but often they just make a product nonworking.

b) Design, layout and technology mismatch errors: Another popular error source is mismatch of electrical design with layout or both of them with a used technology. The first case happens when for some reason the circuit scheme does not match the layout namely in the connection points of different devices. As for the second case, it may be present when design contains parts that cannot be manufactured by the used technology. For example every technology has maximum and minimum dimensions for every component, meaning that if the component is made larger or smaller in schematic, it cannot be fabricated because of the technology limitations. The same applies for layout where components and interconnections cannot be placed nearer to each other than a specific minimum distance.

c) Component mismatch: To wrap up the block design error's group, the last type includes errors which come from the component mismatch. In analog circuits, matching of components is essential because many of them have symmetrical structure like operational amplifier's (OP-AMP) input stage and component mismatch here can degrade the performance of the device dramatically. Other critical matching places are all kinds of biasing and reference circuits where mismatch of the FET's threshold voltage (Vth) and transconductance (gm) can shift the ratio of reference currents and voltages further degrading the circuit's features. The mismatch may be caused by process inaccuracies or by parasitic components which come from interconnection wires. The later can also cause ground fluctuation, meaning that ground point for different devices and components inside the chip can be on different potential levels. This can cause different block to block interface errors which can lead to heavy current leakage.

2.2.2 System design errors

Apart from the errors mentioned in previous subsection which can be also present on system level, there also are purely system errors which do not appear in single blocks unless these blocks are relatively complex. These errors are mainly due to improperly placement. There are connections, wire lines and blocks like the above mentioned reference or audio application circuitry, which are extremely sensitive to any kinds of external distortion or impact. This influence can be caused by other nearby standing blocks especially if they are based on switching clock signals or/and power lines where large currents are possible. The combination of these two features which can be found for example in switching DC-DC regulators gives a source of voltage and current fluctuation along with the radiation of the electro magnetic field. If external disturbance can be shielded off by different shielding materials and package, then internal one is very hard to dispose and if sensitive components are near these distortion centers the failures in the system can occur with the correlation to enabling times of the disturbing blocks.

2.3 Technological Errors

The ever shrinking size of the single components in ICs has raised a great demand on the fabrication technology. Unfortunately there is no possibility for an infinite size decrease for standard mass production technologies mainly because of limitations in lithographic processes. With the conventional photolithographic process most widely used nowadays in analog IC production the emission wavelengths and energies cannot provide a decent resolution for transistor sizes well below 100nm (Fig.4, 5.). For a further successful reduction in size a radically new approaches in manufacturing should be implemented. Even with X-ray lithography it is hard to achieve feature sizes smaller than 20nm [4].

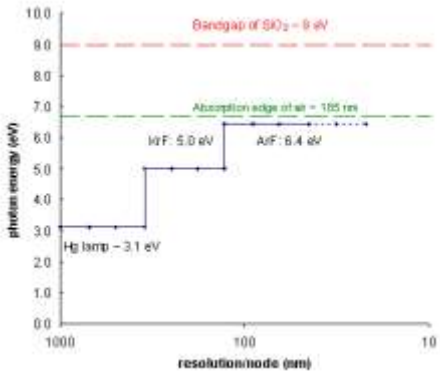

Figure 4. Photolithography photons' energy vs resolution.

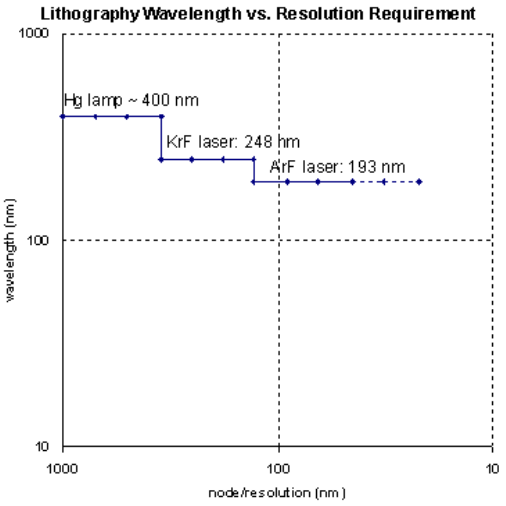

Figure 5. Photolithography photon's wavelength vs resolution.

Meanwhile if return to the conventional fabrication technologies which are mostly used for analog ASICs' manufacture, because for analog purposes very small component sizes are not recommended due to degradation of parameters, then it can be found that almost every process stage has its potential error source. Most important stages and errors produced by them will be overviewed shortly. This will feature impurity diffusion, photolithography**,** etching and film deposition. Other stages such as crystal growth and wafer cleaning represent less interest as the error proof there is more dependent on precision in compliance of technological steps and is not that challenging in the engineering sense.

2.3.1 Impurity diffusion caused errors

Impurity diffusion in IC fabrication is done at rather high temperatures. The most problem causing activities in this case are lateral diffusion and difficulty to create a steep junction on the impurity boundary. This can cause single device dimension inaccuracy like MOSFET's width and length and influence the near standing component parameters (Fig.6.), resulting in inaccurate drain to source resistance Rdson and matching problems discussed in previous section [5,6].

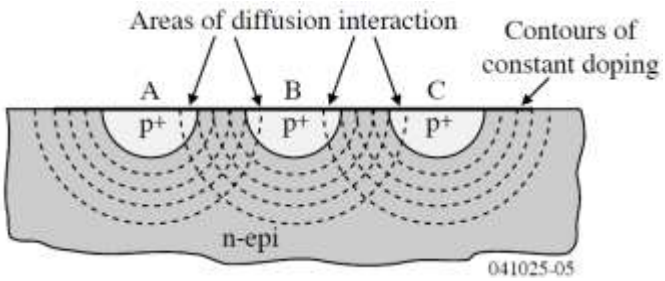

Figure 6. Doping diffusion in n-type semiconductor.

2.3.2 Photolithography caused errors

The most illustrative way to show main danger concerning this process is to take as an example the formation of the MOSFET's gate. When poly for the gate is already deposited, it should be patterned so it can form an appropriate electrode. In order to get precise dimensions a contact printing approach should be used, so that the photomask is at physical contact with the photoresist. However with this type of printing, the wafer is prone to mechanical damage. That is why most often a proximity printing system is used for that where between the photomask and the resist a small gap is left and the radiated light exposes the unprotected photoresist. In this case however some additional resist under the mask can be exposed due to the light diffraction physics, or vice versa not all the needed places exposed if a negative type photoresist is used (Fig.7). This can cause the gate electrode not only to vary from the ideal size, but also to be geometrically non-uniform. The size of gate electrode in its turn can affect the size and operation of the future transistor channel [5, 7].

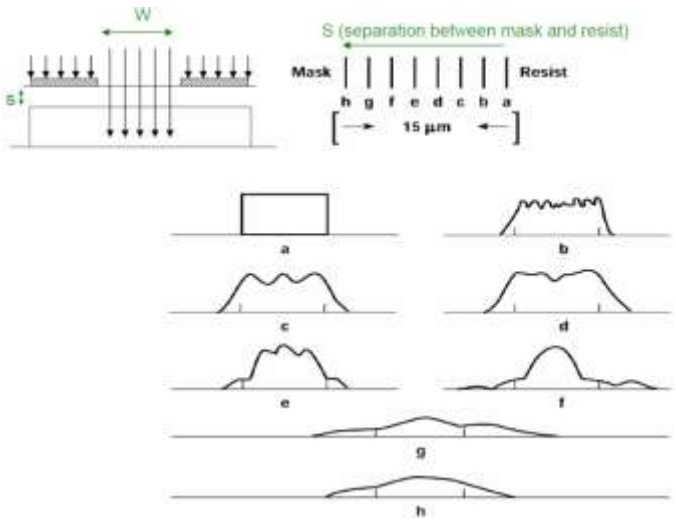

Figure 7. The effect of light diffraction on photoresist pattern formation.

2.3.3 Etching caused errors

Like in previous subsection the same MOSFET's gate example will be used here.

The same effect to further reduce effective gate electrode length can happen when the deposited material for gate electrode is etched. During this process an undercut of the material under the resist can occur like shown in Fig.8. In order to eliminate this parasitic effect, a mechanical etching like ion milling can be exploited. However this technique is associated with different problems in the etched region like re-deposition and trench formation and thus is rarely used. Moreover there is another possible hazard from etching. The thing is that not everywhere the velocity of etching is uniform. The film is etched faster in clear areas and slower near the resist boundaries, thus the etching gradients in such places will be different leading to another mismatch source [5, 8].

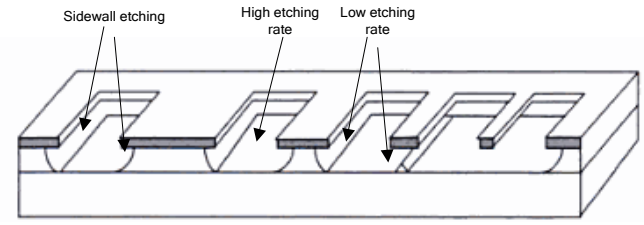

Figure 8. Etching hazards.

2.3.4 Film deposition caused errors

If take the same example with formation of the MOSFET's gate, the possible error source from film deposition is not in causing inaccuracy in the component dimensions but rather in its parameters, namely in its threshold voltage. This can be due to poor morphology of the gate poly, which can lead to variations in contact potential and hence the threshold voltage. Poor morphology is often caused by particle formation during chemical vapor deposition (CVD) process at atmospheric pressure [5].

III. Error Reduction Techniques

This chapter will be dedicated to the main techniques for reduction of the errors discussed in the 1st part. The same order of topics will be kept in order not to mix all up and make it more complicated to understand. Consequently first ways to overcome physical error sources will be discussed followed by design and technological ones.

3.1 Physical Error Cancellation Techniques

As it has already been said physical errors caused by external impact can be neutralized by using different kinds of shielding materials including in package manufacture and are not of interest from IC design point of view. Thus the main attention will be focused on internal heat and noise sources.

3.1.1 Temperature based errors' reduction

There are several ways to fight extensive heat dissipation. One of them is to make device larger so they can dissipate more heat without going into breakdown region. This works well for all conditions not considering the source of the heat generation. However this is not very good from chip size point of view and it does not protect from component parameter degrading. In order to overcome those, a different approach should be considered with separation into groups by generated heat type taken from the 1st chapter.

a) Heat generated by physical discontinuity of applied voltage and current: The most effective way of fighting this error source is implementing some layout techniques in order to spread the heat on a possibly larger area thus limiting the possibility for hot spot occurrence. For example in Fig.1 one possible solution is to move connections on both sides of the channel to the opposing corners like in Fig.9. Such technique helps to achieve a more balanced temperature distribution in the channel (Fig.10.) [6].

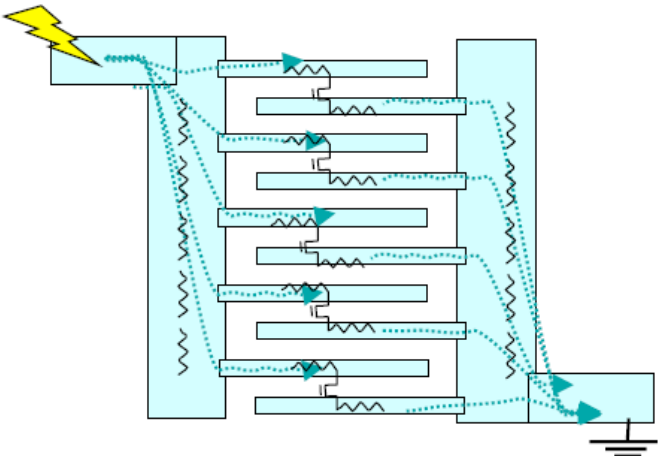

Figure 9. MOSFET layout with hot spot reduction

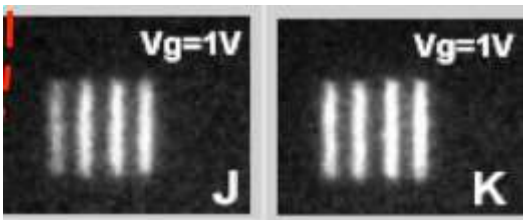

Figure 10. Current distribution in MOSFET

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b) Heat generated by other blocks: This is a much more complicated thing which is not that easy to get over. The way the heat is radiated from blocks is hard to predict as well as the way it interacts, because most often the enabling and disabling of the blocks is caused by external application factors and is not well periodically set. That is why there are no standard solutions to that problem, and every product must be treated separately. One way to reduce the negative effects here is to lower the heat radiation of the single blocks with techniques presented earlier. Another way is to try and synchronize the operation of different blocks in such an order that the most temperature sensitive blocks do not operate simultaneously with the blocks that dissipate much heat likewise it is not recommended that a lot of the latter ones are working together in order to keep chip temperature on a sustainable level. At the same time it is better that these powerful heat sources are kept at possibly greater distance from each other. And again the implementation of special layout techniques like segmentation and cross-coupling of sensitive elements and a well organized placement of them in relation to the main heat generation elements (Fig.11) help to reduce the effects of the temperature gradients inside the chip considerably.

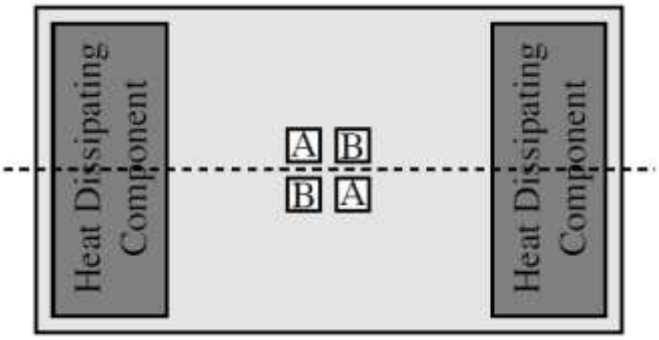

Figure 11. Current distribution in MOSFET

3.1.2 Electrical noise based errors' reduction

The main techniques for noise reduction and thus the reduction of the noise caused errors lay in electrical design and technological planes. One common technique for that is using different kinds of filters together with other design tricks. Here these methods will be overviewed with every noise type considered in 1st part.

a) Thermal noise: There is not much to do with this error source as thermal noise is always present when temperature is above 0K. So noise can be reduced by reducing temperature; however in most cases it is not very practical, so this method often cannot be used in application. As it has already been said the frequency spectrum of thermal noise is flat, so by filtering it is not possible to get rid of this noise completely, however it is possible to filter out the unneeded frequencies i.e. the frequencies that do not contain the useful signal by either lowpass, highpass or bandpass filters of the necessary order. The higher the order of the filter used the steeper the cut-off slope and the better the rejection in the stop bands. Although the noise in the signal band is still present and cannot be

reduced, by filtering the out of band noise the entire noise spectral density RMS value becomes lower which benefits the entire circuit's operation. In some devices however it is not possible to use noise filters at the output due to the load driving limitations. This is valid for example in power management devices like voltage regulators. In this case it is possible to filter the main noise producing circuitry and then buffer the result with the use of low noise architecture like it is done in low noise LDO in Fig. 12 [9].

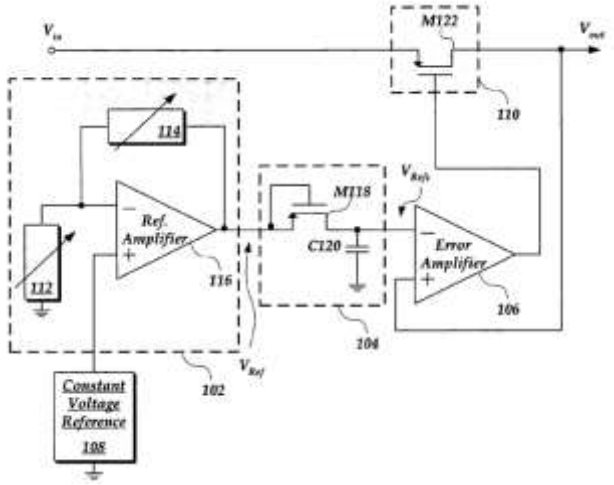

Figure 12. Low noise LDO architecture

b) Shot noise: Here, similarly to thermal noise case application of noise filters effectively reduce noise PSD. Additionally it is possible to reduce the noise affect on the useful signal by increasing the signal magnitude. As it was shown in 1st part, shot noise can affect the operation of a circuit only at low useful currents because from (4) the useful current grows at a significantly higher gradient than the noise portion. Thus if the signal magnitude is comparatively high, the effect of the noise is reduced although the absolute noise value is increased.

c) Flicker noise: As it is seen in Fig. 2 flicker noise is significant on lower frequencies. So in order to filter out this region, the signal band can be shifted into higher frequencies together with the use of a band pass filter. In this configuration the previous 2 noise types are also reduced.

d) Burst noise: It is supposed that burst noise is caused by contamination of the semiconductor. So the best way for fighting this is to use a more clean process and use techniques similar to those used for reducing technological errors.

The best way to implement a low noise design in analog IC's including ASICs is to combine all of the methods stated in this section, so all types of noise sources are kept under control.

3.2 Design Based Error's Reduction

This section will be fully dedicated to the topic of how to eliminate or at least significantly reduce errors that come from design faults on both block and system levels. Here the subsections that address the consequent error sources will be presented. The first 3 subsections will be dedicated to block level design errors and the last one to specific system errors.

3.2.1 Calculation errors reduction

There are several standard procedures and methods to overcome these. First of all before releasing the product to fabrication or block to further integration, every schematic must be simulated in order to find out if the designed parameters correspond to the specified (calculated) ones. The simulation is usually done with different inputs that correspond to the entire application range, ambient conditions (temperature, external component equivalent values etc.), types of analyses (static, dynamic, transient etc) so that the widest range of possible errors would be checked. Although simulation results can significantly reduce calculation errors, they cannot absolutely remove them, because no simulator can include all components physical features thus the result received in simulation can differ from reality (Fig. 13). So even with such a wide coverage of circuits' operation it does not give full confidence that all the specified features will be met. That is why after all the simulation is done and the chip is released from fabrication, it must be first evaluated to check all the needed parameters before giving the product to the customer. The evaluation environment must be as close as possible to the one used in customer's application [10].

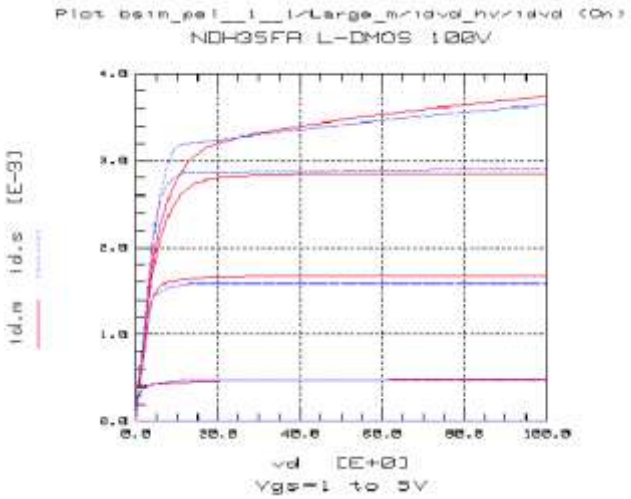

Figure 13. Simulated (blue) vs measured (red) Ids-Vds characteristics of an N-type HV transistor

3.2.2 Design, layout, technology mismatch error reduction

This error can be completely neglected by obeying design and layout rules. These rules define the limits for component sizes and distances between each other and interconnection wires that can be used without causing production errors. Every technology has its own rules and many modern CAD tools have possibility to check whether these rules are abused. So by using these tools and performing the needed checks it is possible to neglect the effects of these errors.

3.2.3 Components mismatch error reduction

All possible actions protecting from these errors are done in layout. In order to minimize the effects of ambient and process factors on transistor couples that should be well matched the following steps can be taken. First, each transistor is divided into equal number of equal pieces. After that these pieces are mixed up and put together in such an order that the mentioned factors affect both FETs in the same way. One possible way to do that is common-centroid layout like shown in Fig. 14.

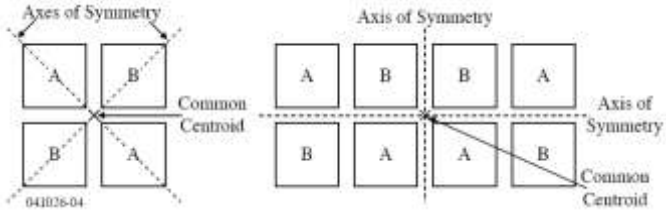

Figure 14. Common centroid layout

As for possible reduction of parasitic component effects the best way is to try to make all wires that come into the same node possibly the same size or at least they should not be interconnected for several times, as this can bring to additional voltage drops for some wires. As an example the case with different ground potentials can be examined in Fig. 15. [6].

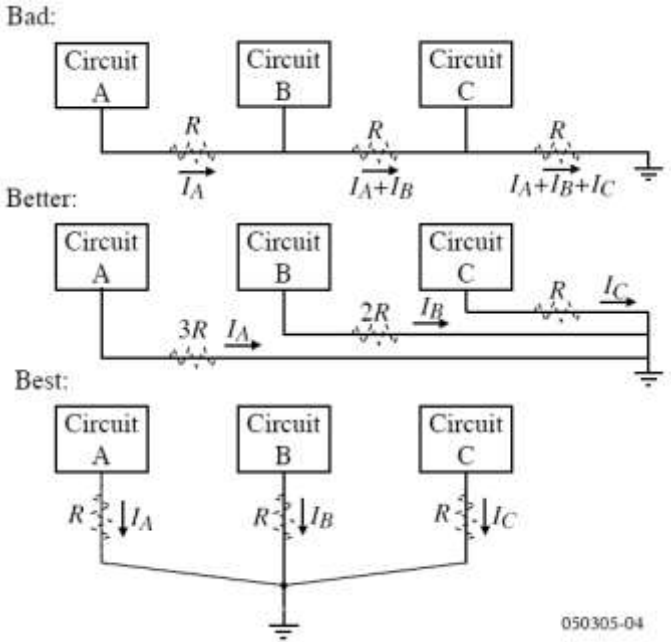

Figure 15. Layout for minimization of the parasitics' effects in ground connections

3.2.4 Placement error reduction

In order to make the correct placement of the components so that they do not affect each other badly a system design algorithm called a top-down approach can be implemented. Unlike the bottom-up approach where small components act as building blocks for the entire system, in top-down algorithm first the behavioural models of all blocks are placed inside the chip. The system's behaviour is simulated to find out what is the best placement of the blocks and operational timing. And only after the ideal combination is found the block models are replaced with real blocks followed by a complete simulation of the entire system.

Additionally to the top-down approach, for sensitive elements and signal paths could be shielded and isolated from the noisy lines and components. This can be done in two ways. First sensitive wire lines can be put into a grounded shielding of an upper and lower level metals. Second, if the technology allows, it is possible to isolate the entire sensitive block like a bandgap reference using a buried layer inside the substrate. This way even the substrate induced distortion e.g. from a switching DC-DC regulator will not propagate into the reference block.

3.3 Technological Errors' Reduction

In this section the main possible techniques for reduction of technological errors introduced in the first part will be discussed.

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3.3.1 Impurity implantation errors' reduction

One common technique to reduce the lateral diffusion of the impurity atoms and create a steeper and more controllable junction is to use a different approach from diffusion, called ion implantation. With this process the dopants are introduced by ion beam where ions are driven to high velocities. This way by regulating the speed of the ions it is possible to accurately regulate the depth and concentration of implant and as the overall temperature is significantly lower than in diffusion case the lateral movement of the ions is minimal. One negative side of this process is that when the impurity ions penetrate the wafer they can cause damage to the crystal lattice. This damage should be repaired after the implantation is done. This is obtained by a high temperature anneal during a very short time period.

3.3.2 Photolithography errors' reduction

From the earlier discussion it has been found out that contact printing is not recommended due to physical contact and the liability of proximity printing is the diffraction issue. So in order to have a high resolution pattern, one solution is to place the mask very close to resist but without the physical contact. This can work well when the devices are reasonably big. In this case the diffracted light portion will be small. The same effect brings the usage of the higher energy light source like it was said in the error discussion part. Additionally there is one more solution to this problem. It is possible to use a different printing technique called projection printing. With this technique two collecting lenses are placed one between light source and mask and second between mask and photoresist (Fig.16). In this case the light is exposed not to entire wafer simultaneously but to a part of it at a time. This way time consumed on a single wafer is increased but the resolution is improved significantly which is much more important in the safety critical applications [7].

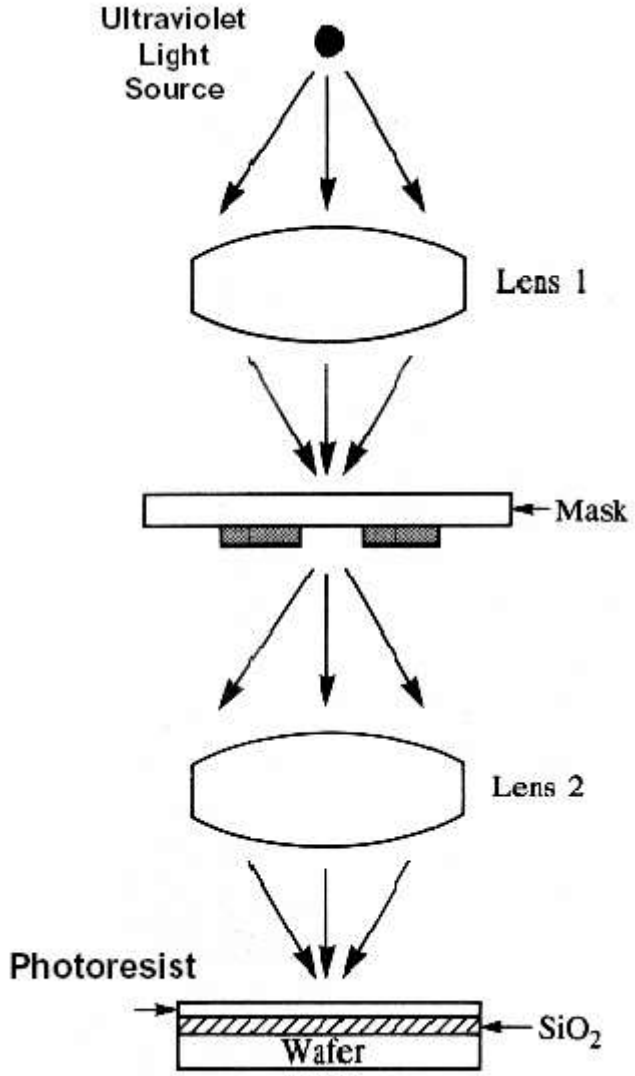

Figure 16. Projection printing.

3.3.3 Etching errors' reduction:

The reduction of useful material undercut is achieved by combining both of the mentioned etching techniques into a high pressure plasma technique. In this process apart from chemical reactions, etching is supported by ion bombardment hence mechanical etching takes place and formation of the sidewall passivating film due to vertical orientation of bombardment ions reduces the undercut. The inconsistency in the etching rates in different junction densities is reduced by introduction of some dummy elements in layout which are not used in circuit's operation, but help to achieve a uniform etch rate like in Fig.17. [6]

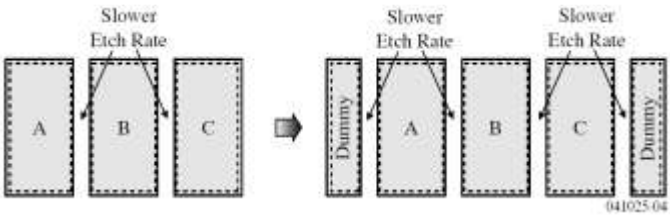

Figure 17. Layout for a uniform etching.

3.3.4 Film deposition errors' reduction

The main idea of improving deposited film morphology and hence decreasing the accompanied errors is to minimize particle formation. This can be successfully accomplished by caring out the entire process in vacuum pressure, where particle concentration is significantly lower.

3.3.5 Summary of the technological errors' reduction

Although the above mentioned techniques significantly lower the possible technological errors, it cannot guarantee their absolute absence. That is why in order to guarantee the product's specified operation and parameters, every chip coming out of fabrication must be tested to comply with specification. This test is called an automated production test and is different from evaluation process discussed earlier. In evaluation case the main activity is to find errors, their sources and purpose methods for improvement, in production test case there is no time for a complete analyses of chip's operation that is why only the main specified parameters are checked to be in the needed limits. It is a very quick test performed automatically based on the special program developed for each product. A design for testability approach in the chip's design stage can improve accessibility to different blocks of a complicated ASIC system and thus decrease test time considerably. So it is recommended that designers pay more attention to testing aspect in both block and system design.

IV. CONCLUSION

In current article the main error sources in analog ASIC development were analyzed. This included physical, design and technological errors, which build up the main possible error band for these products. Furthermore methods for minimizing and overcoming all of these errors were overviewed and analyzed.

One of the main ideas of the paper was to build up the knowledge that can be used in development of methodology for dependable analog ASIC products. From the above made discussion it can be clearly stated that the most correct approach towards realization of this goal is to combine all of the mentioned techniques into a single, well performing and communicating mechanism, because by isolating different processes and trying to solve them independently, a possibility to mask the errors formed in other parts and from other sources exists.

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